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Installation and Commissioning of the ATLAS Liquid Argon Calorimeter Read-Out Electronics

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Abstract

The cryostats of the ATLAS LAr calorimeter system are installed in the ATLAS cavern since several years. Following this, an effort to install and commission the front-end and back-end read-out electronics as well as the timing, trigger and control electronics (infrastructure, crates, and boards) has been ongoing and is finished now, in time for the cavern closure. Following cautious procedures and with continuous testing-campaigns of the electronics at each step of the installation advancement, the result is a fully commissioned calorimeter with its readout and a small number of non-functional channels. The paper will give a general overview of the installation and refurbishment campaign of the ATLAS LAr calorimeter electronics. Different problems observed and addressed will be discussed. It will describe noise studies that have been performed and shortly review the solutions implemented to reduce noise.

I. INTRODUCTION

The ATLAS experiment [1] at the LHC is a general purpose detector designed to exploit the full physics potential of the LHC at CERN. The collider will produce proton-proton collisions at a centre-of-mass energy of 14 TeV.

Liquid Argon (LAr) sampling calorimeters [2] are used in ATLAS for all electromagnetic calorimetry covering the pseudo rapidity interval < 3.2, as well as for hadronic calorimetry from 1.4 to the acceptance limit of 4.8.

The LAr calorimeters consist of four sub-detectors and are contained within three cryostats as shown in figure 1. The central cryostat houses the electromagnetic barrel calorimeter (EMB), while each end-cap cryostat contains an end-cap electromagnetic calorimeter (EMEC), 2 hadronic end-cap wheels (HEC) and a 3 wheels forward calorimeter (FCAL). In total 182468 calorimeter cells are to be read out.

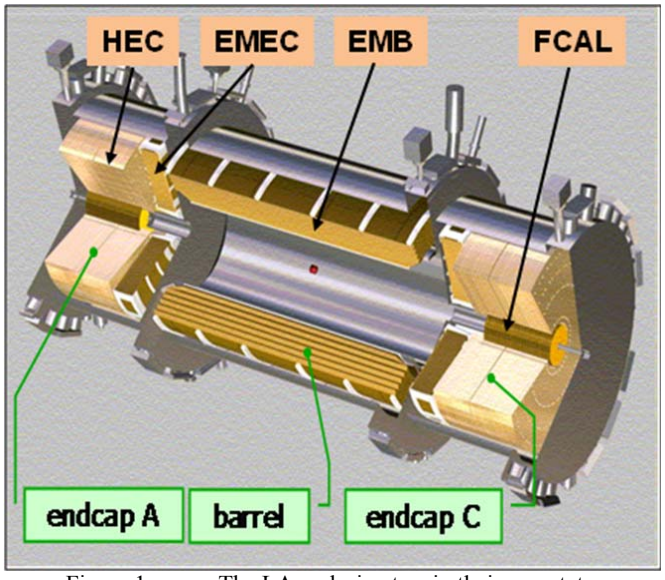

Figure 1: The LAr calorimeters in their cryostats.

A choice of common electronics for all calorimeters standardizes the hardware to simplify the maintenance. The HEC nonetheless uses cold preamplifiers.

The main tasks for the readout electronics are:

- To measure, for triggered beam crossings, the energy deposit in each calorimeter cell to better than 0.25% at high energy. The dynamic energy range will cover a maximum of 3 TeV down to a lower limit of 10MeV. The readout should proceed without any dead time up to a trigger rate of 75 kHz.
- To provide the trigger system with the energy deposited in trigger towers of size .1in pseudo rapidity ×.1in phi. The trigger processor combines the information from all ATLAS sub-detectors to deliver at the 40 MHz bunch crossing rate a yes/no decision to read out the detectors.

II. THE READOUT ELECTRONICS

A. Generalities

The readout architecture is sketched in figure 2.When a charged particle traverses and ionizes the liquid Argon in the gap between a LAr electrode and an absorber, an ionization current is measured on the readout cells of the electrodes due to the drift of electrons. The pulse height is proportional to the energy deposit of the particle.

The analog signal is received, pipelined and digitized by the front-end boards (FEB) mounted directly on the detector. The FEBs send the digitized pulse via optical links to the Read Out Drivers (ROD) which are installed in a radiation-free area (USA15) next to the detector cavern (UX15).

Summation of the analog signals is also formed, mostly in the FEBs or in the Tower Builder Boards (TBB) or Tower Driver Boards (TDB) for the HEC, but also in some cases in the receiver system (barrel-EC transition region and FCAL) to build primitives which are sent to the L1 trigger interface to be treated by the Level-1 calorimeter processor.

Each ROD receives the data from up to 8 FEBs and processes the signals of up to 1024 detector cells (128 cells per FEB). For each cell, it will calculate the energy deposited but also the time of the deposition and a quality factor for cell with a high energy deposit, using an optimal filtering algorithm [3]. The ROD sends these results and sometimes

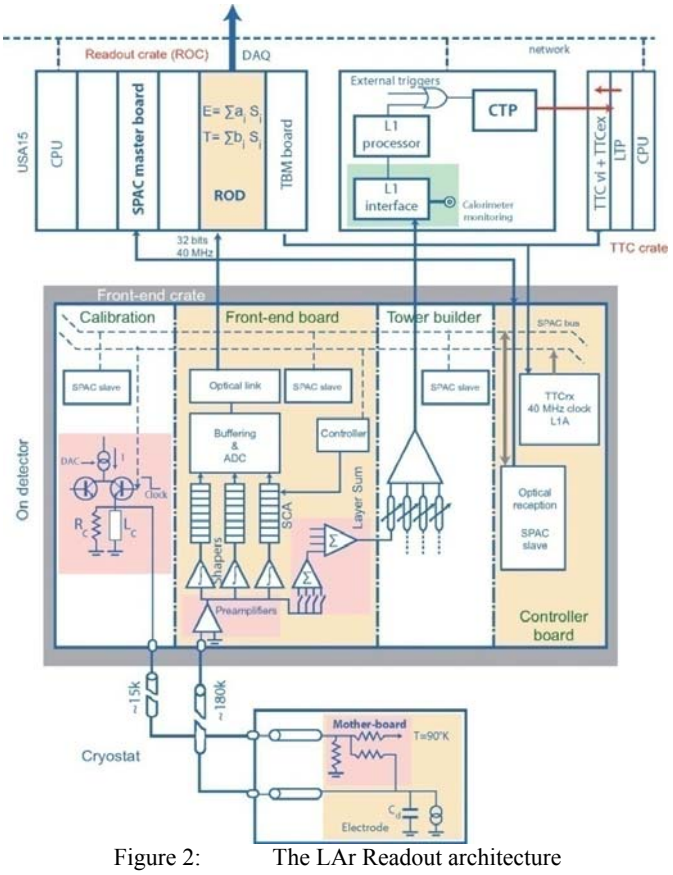

Figure 2: The LAr Readout architecture

also the raw data through 4 optical links housed on a Transition Module (TM) at the back of the ROD, the S-links, to the Read Out Buffers (ROBs) hosted on PCs (ROS).

The LAr readout elements need the bunch-crossing signal (40.08 MHz BC clock) from the LHC machine and the Level-1 accept signal (L1A) from the trigger system. In addition, to synchronize all the readout elements, the LHC provides once per turn the Bunch Counter Reset signal (BCR) used to reset the Bunch Counter Identifier (BCID) in each readout element at a fixed time within the LHC cycle. The Timing, Trigger and Control (TTC) system distributes these signals to both front-end and ROD system electronic via optical fibers.

B. The Front-End electronics

As was shown in figure 2, the FE system [4] includes front-end boards (FEB) which perform the amplification, shaping, sampling, storage, digitization, and readout of the calorimeter signals. Calibration boards inject precision calibration signals, and Tower Builder Boards and Tower Driver Boards produce analog sums for the L1 trigger. The various boards in the front-end crate (FEC) require the TTC signals for proper operation. In addition, most of the boards need to be configured and monitored. A custom serial link known as SPAC (Serial Protocol for the ATLAS Calorimeters) is used for this purpose. Controller boards (CONT) installed in the FECs are used to receive and distribute the TTC and SPAC signals to the various FE boards.

These boards are housed in 58 front-end crates which are divided in 2 half front-end crates (HFEC) in terms of functionality (FCAL has 2 HFEC but in 2 different crates).

The total number of boards and their distribution on the LAr detectors is summarized in table 1

Table 1: Number of FE system boards

HFEC Type	HFEC	FEB	CALIB	CONT	TBB	TDB
EMB	64	896	64	64	64	-
EMEC Standard	32	416	32	32	32	-
EMEC Special	8	136	16	16	24	-
HEC	8	48	8	8	-	16
FCAL	2	28	2	2	-	4
Total	114	1524	122	122	120	20

The low voltage power required by the FE electronics is delivered by a low voltage power and distribution system made of 58 identical partitions. AC-DC primary power supplies (PS), fed from the 400 VAC three-phase network in the ATLAS pit and organized in racks in USA15, deliver 280 VDC and 10-11 A to low voltage power supplies (LVPS) made of DCDC converters mounted on the detector adjacent to the corresponding FEC.

For each of the 128 detector cells of a FEB, the signal is first subject to several stages of analog processing. Preamplifier hybrids amplify the raw signals, which are then split and further amplified by shaper chips to produce three overlapping linear gain scales, with gain ratios of ≈ 10. Each signal is subject to a fast bipolar CR-$(RC)^2$ shaping function.

The shaped signals are then sampled at the LHC bunch crossing frequency of 40 MHz and stored by switched capacitor array (SCA) analog pipeline chips, which store the signals in analog form during the L1trigger latency.

For events accepted by the L1 trigger, typically five samples per channel for physics but up to 32 for commissioning, are read out from the SCA using the optimal gain scale, and digitized using a 5 MHz 12-bit Analog-to-Digital Converter (ADC) common for 8 channels. The digitized data are formatted, multiplexed, serialized, and then transmitted optically out of the detector to the Readout Driver (ROD) in USA15 via a single 1.6 Gbps optical link per FEB.

C. The Back-End electronics

The BE electronics [5] is composed of three systems: the ROD which is the core of the BE, the TTC and the Level-1 receiver.

1) The ROD system

As can be seen in figure 2, the ROD system includes ROD boards to calculate the energy, time and quality factor from the digitized samples sent by the FEBs, TM boards housing the S-links, SPAC Master boards to control and monitor the HFECs and a TBM board to receive the TTC optical information and distribute it electrically to the ROD boards in the crate. It also collects the RODs busy signals in the crate and sends the OR of them to the TTC system.

These boards are housed in 16 9u VME64x crates each controlled by a VME Processor.

The system has been split in 6 partitions each corresponding to a slice of the LAr detectors.

Table 2 summarizes the number of crates and boards for each of the partitions.

Table 2: Number of crates and ROD system boards

Partition	Crate	ROD	TM	SPAC M.	TBM	CPU
EMB-A	4	56	56	8	4	4
EMB-C	4	56	56	8	4	4
EMEC-A	3	35	35	6	3	3
EMEC-C	3	35	35	6	3	3
FCAL/HEC-A	1	5	5	2	1	3
FCAL/HEC-C	1	5	5	2	1	3
Total	16	192	192	32	16	16

The ROD board receives the TTC signals and has 8 DSPs for doing the calculation on the data received from the 8 FEBs (1 per FEB). For each event accepted by the Level-1 trigger (L1A), it will generate the corresponding BCID and L1ID. It will also directly receive from the TTC system the Trigger type and transmit them to the 8 DSPs. For each event the DSP will match the data coming from the FEB with the TTC information (BCID), calculate the energy and if needed the time and quality factor for each of the 128 cells from the 3 to 32 samples received. The results of the calculation and also raw data (above a configurable threshold per cell, the raw data will be written out as well) of 2 DSPs will then be merged and sent to the TM to be output on one of the 4 optical links, the S-links, to the Read Out Buffers (ROBs). The reception, matching calculation and transmission must be done within 12 microseconds which is the average time available for a mean L1A rate of 75 KHz. If the DSP cannot accept anymore events, it will set a busy signal to pace the Level-1 Trigger.

2) The Timing, Trigger and Control system

The Timing Trigger and Control (TTC) system distributes the different timing and control signals to both front-end and ROD system electronics via optical fibers. This includes the LHC clock (BC), the L1A, the BCR and Event Counter Reset (ECR), the Trigger type as well as more specific command to some modules like the calibration command for example.

The 6 LAr detector partitions each have their own TTC system using a Local Trigger Processor (LTP) in order to run independently when needed. They are housed in 3 6U VME64x crates. Each crate houses 2 partitions covering the same type of detector (Barrel, EMEC, FCAL/HEC) which can be run together under the control of 1 LTPs acting as a master, the other as a slave. On top of that a structure housed in a 4th crate with a special LTP and 4 Local Trigger Processor Interfaces (LTPI) allows all or some of the partitions to be run either under the control of the Central Trigger Processor (CTP), the special LTP or other subsystems (Tiles Barrel Hadronic Calorimeter and Level1 calorimeter Trigger).

Within a partition, The ROD Busy module (RODB) collects the busy from the different ROD crates and transmits a partition busy to the LTP to pace the level-1 trigger generation. When in master mode, the LTP generates all the timing, trigger and control signals, while in other modes it gets the signals from higher in the chain. They are then encoded in the TTCvi and sent on optical links by the TTCex. Optical couplers 1 to 32 (OC32) or 1 to 16 (OC16) provide the necessary optical fan out. For the 6 partitions a total of 212 fibers are connected to the front-end (2 per HFEC, 1 being a spare) and 16 fibers to the ROD electronics. Table 3 summarizes the number of elements for each partition and the control structure.

Table 3: Number of TTC elements

Partition	RODB	LTPI	LTP	TTCvi	TTCex.	OC16	OC32
Control	-	4	1	-	-	-	-
EMB-A	1	-	1	1	1	-	2
EMB-C	1	-	1	1	1	-	2
EMEC-A	1	-	1	1	1	1	1
EMEC-C	1	-	1	1	1	1	1
FCAL/HEC-A	1	-	1	1	1	1	-
FCAL/HEC-C	1	-	1	1	1	1	-
Total	6	4	7	6	6	4	6

3) The Level-1 receiver system

The Level-1 receiver system is not described in this paper.

III. The HV system

The HV system provides the drift voltage across the LAr gaps in the calorimeters between electrodes and absorbers. The LAr calorimeter cells are connected to about 4700 HV supply groups, distributed roughly equally among each of the three cryostats. Each of this group is connected to a single HV channel. A total of 157 commercial 32-channel HVPS modules are used, mounted eight to a subrack in 20 subracks. A summary of the HV module count with channel parameters is listed in table 4.

Table 4: List of HV modules used for the various parts of the LAr calorimeter system.

Detector	Operating Voltage (V)	Max. Current (mA)	Nb. of 32-Channel Modules
EMB	2000	75	53
EMEC	1000 to 2500	200	56
HEC	1800	75	32
FCAL	250, 375, 500	6000	14
purity detectors	2500	75	2

IV. Installation and commissioning Experience

A. Generalities

The procedure was to install hardware and test it as soon as possible in a stand alone mode. Then to leave it running, integrate it and use it as much as possible.

Electronics for the front-end was installed and tested one crate at a time with stand-alone tests including pedestal and calibration runs using dedicated acquisition systems.

Electronics for the back-end was installed one crate at a time and tested one half crate at a time with a specific injector system to replace the FEBs and a FILAR based readout

system to replace the ROBs, which were not yet connected. TTC signals were provided by the final TTC system.

As soon as these elements were tested and interconnected, they were integrated into the global acquisition system.

Since then the detector has been commissioned continuously with the available readout system doing pedestal, calibration and cosmic runs to verify its behaviour and stability.

B. The Front-End electronics

Installation of the front-end electronic started in summer 2005 for the barrel and in May and August 2006 for the 2 end-caps respectively. All the crates for the Barrel had been tested in September 2006 and December 2006 for the end-caps, but the complete set of power supplies after refurbishment were only available in August 2007. The FEB also needed refurbishment and this was accomplished between July 2007 and March 2008 for the Barrel, end-cap C and end-cap A.

The first time we could read the full LAr detector was in May 2008, a short time before the closure of the apparatus.

Tests of the FE crates were done with 2 stand alone read-out systems located in USA15: One for the barrel and the other for the end-caps. In both cases a LVPS was moved from crate to crate together with a cable made of 48 fibres between UX15 and USA15. As there was no cooling infrastructure for the barrel, the FEBs had to be tested one at a time. For the end-caps a standalone cooling system was used and a full FE crate was tested in a single pass using a read-out with 4 RODs and standard TDAQ software. Pedestal runs and calibration runs were sufficient to show all defects like bad shapers, damaged calibration lines, dead FEB channels…

All FEBs had to be refurbished, initially because a mistake had been found in the level adaptation of 2 signals between different ASIC technologies. There was an increased risk of long term failure for these components. This was a good occasion to correct another problem which had been apparent only on some boards. Some shapers had their timing constant changing over time due to uncertain disconnection of a resistance network used to precisely set this time constant. This network was adjusted at the time of testing of the chips by burning fuses on the IC which turned out to suffer from partial reconnection over time. By cutting the pins corresponding to the burnt fuses for each shaper, this problem was definitively solved. As a further surprise, when getting the boards out, corrosion was found on some boards. This was due to a bad cleaning process after repair of some boards during production tests. About 50 boards were damaged beyond repair while the others could be recovered after a new cleaning. A new batch of 40 boards is being produced for spare.

The LVPS have been plagued by failures right from the beginning. In summer 2006 a task force was setup to do a deep review of the LVPS. It led to many modifications and component replacements in the design in order to use them for the first years of LHC operation. All LVPS were refurbished between spring and august 2007. All have been working since, though one has lost its redundancy. Following the review, a backup project has started with 2 companies to produce new designs and prototypes, as the reliability of the refurbished power supplies cannot be guaranteed for the lifetime of the LHC operations. In June 2008, when the barrel toroid was turned on for the first time, it was observed that the induced magnetic field was too high in some positions of the end-caps LVPS. An important effort with measures and simulations showed that the installed shielding was not sufficiently covering the magnetically sensitive LVPS. New shielding plates were manufactured and installed in very tight and hardly accessible positions.

C. The Back-End electronics

Installation and tests of the back-end electronics started in August 2005 and were finished in April 2007 for the RODs and in June 2007 for the fibre connections to the ROBs.

The injector system used for the tests consists of 6 9U VME 64x modules with 5 outputs each. 1 to 2 optical splitters on each output provide a total of 60 FEBs equivalent output needed to test half a ROD crate. The readout of the RODs was done by 3 ROS PCs equipped with 7 FILAR boards providing the 28 readout inputs needed. The Injector generates data with the same format as the FEB when receiving L1A. A comparison of the injected data with the read-out data is done to validate the half crate.

Front-end fibres were then connected when available, followed by the fibres to the ROBs. Final commissioning using FEBs and ROSes could then start. This commissioning has been going on since June 2007 until the first beam.

The major problem encountered was the commissioning of a full ROD crate using FEBs and ROBs with a high L1A rate (>40 KHz) and transferring the raw data. In this mode, transfers on all ROD modules within the crate are almost synchronous, paced by the busy of the system. This generated huge current surges on the 3.3 V power supply which is connected to the crate through a 1 meter long cable. It produced a voltage oscillation which triggered the overvoltage protection circuit of the power supply and shut it down. A solution was found by doubling the cable in order to reduce the inductance and by adding a big 3.3 mF capacitor on each of the ROD boards to have a better current reservoir.

With these modifications, in the same conditions, the current surge was reduced from 30 A to less than 10 A and the voltage oscillation from 300mV to 50 mV. We haven't seen any problem since these modifications, whatever the conditions of operation.

D. The Timing Trigger and Control

Installation of the TTC system in USA15 started in September 05 as soon as the rack infrastructure was available. It was completed in November of the same year except for the control structure (LTPIs) which was added in May 2008.

The TTC system was first connected to the ROD system electronics and used for the ROD system commissioning. Connection to the front-end electronics was finished in August 2007 allowing commissioning tests with both front-end electronic and ROD system.

There was never a specific commissioning of the TTC system. Rather functionalities were progressively used and tested when needed for the commissioning of the detectors.

Problems were only discovered when we started to use the system at high speed in long term tests in fall 2007.

The first problem to observe and understand was that a L1A could occasionally go through when the Busy was present. This was tracked down to a fault in the ROD Busy module. A glitch of a few ns could be observed on the TTL open collector output of the Busy when there was a VME access to the status of this module. It was large enough for the LTP to be able to produce a L1A if it happened at the wrong time. The cure was to use the NIM output which filters this glitch in the conversion from TTL to NIM.

The second problem was related to a few corrupted events received from the FEBs by the RODs in long runs (days) and at high rate L1A. This problem took 6 months to understand as it implied a very complex mechanism.

VME accesses to the status register of the LTP can provoke a very small glitch on the clock output of the LTP (1-2ns) when at the same time there is a transition on the LTP internal orbit signal and the internal LTP clock has a different logic level than the incoming CTP clock. This glitch should not have any effect as it should be filtered by the PLL in the TTCex. But this glitch, when present at the input of the Analog Device TTCex phase comparator of the PLL, stops it for 350 microseconds. This is an unexpected behaviour that the manufacturer has not been able to explain. As a consequence the TTCex output clock starts shifting in order to recover the lock process which takes a few milliseconds. This provokes a corruption of the data sent by the FEBs on the link and at a later stage an unlock of the QPLL in the FEBs which then needs a further 400 milliseconds to recover. During all that time data can be more or less corrupted as the FEB and ROD clock is shifting permanently.

The clock glitch was suppressed with a new version of firmware for the LTP. The TTCex was not modified as the correction proposed by Analog Device has not shown any improvement.

V. Noise related issues

Noise correlated to the Tile Hadronic calorimeter power supplies with a frequency peak at 17 MHz had been observed when operating a large fraction of their system. The noise was entering the LAr system by the feed-through heater cables and by capacitive coupling affected channels on the nearby cables in the FEC supports on the cryostats. These heater cables were equipped with filters efficient only up to 10 MHz. Additional filter boxes have been added. Tile power supplies have also been modified to incorporate additional output filters.

Noise bursts have been observed in cosmic and pedestal runs. It was originally identified with the help of the so called OddCellMonitoring software tool. The original pedestal of each channel or cell have been measured and recorded. With a perfect Gaussian noise distribution (width of σ noise) we would expect about 0.27% of the cells to be over 3 σ noise away from the pedestal in a given event. If a certain channel is more often above this threshold, it is easily identified. Looking at the L1 interface output with a spectrum analyser where many cells are added, we see noise peaks in the range 3.5 to 6 MHz. Looking at the signal with a scope we could see the noise increasing with a periodicity of 250 microseconds. The source of this noise was not identified but the path to get into the LAr detector was shown to be via coupling between the outer shield of the HV cables and the internal cables. In order to avoid grounding loops between the detector and the back-end electronics very strict grounding rules have been agreed upon and implemented. The shield of the HV cables was only connected on one end (USA15). This noise was suppressed by adding a 1 microfarad capacitor between the outer shield of each HV cable and the cryostat. This was done at the level of each HV filter box located on the cryostat.

VI. Conclusion

The back-end electronics is now fully commissioned and operational with no dead channel as it is easily accessible in case of failure.

The front-end electronics which is now not accessible is also commissioned and operational, with a few dead elements. Recently, one $1/8^{th}$ of the HEC calorimeter could not be readout due to the failure of a power supply for the cold preamplifiers. Also 7 FEBs out of a total of 1524 are not transmitting their data to the BE but are operational for the trigger. These problems will be fixed during the next shutdown.

The detector has 100% of its HV channels working with about 6% of them operated at a reduced voltage but still producing a usable signal. 0.5% data channels have minor problems like increased noise or damaged calibration lines.

The readout system is now very stable. Cosmic data has been taken over the last 2 years together with other ATLAS sub-detectors. The calibration constants which have been monitored over a few months are stable at better than 0.1%. The ATLAS LAr system is ready to record the first LHC beam events.

VII. References

[1] The ATLAS Experiment at the CERN Large Hadron Collider The ATLAS Collaboration, G Aad et al 2008 JINST 3 S08003

[2] ATLAS LAr Collaboration, ATLAS Liquid Argon Calorimeter Technical Design Report, CERN-LHCC-96-041,

[3] Signal processing considerations for liquid ionization calorimeters in a high rate environment,W.E. Cleland and E.G. Stern, Nucl. Inst. Meth. A 338 (1994) 467.

[4] ATLAS liquid argon calorimeter front end electronics N J Buchanan et al ,2008 JINST 3 P09003

[5] ATLAS Liquid Argon Calorimeter Back End Electronics A. Bazan et al, 2007 JINST 2 P06002.